

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of : CHUNG, David B.

Assignee: Intel Corporation

Application No.: Not assigned

Filed: October 16, 2003

Examiner: Not assigned

Group Art Unit: Not assigned

For: SPATIALLY INTEGRATED DISPLAY AND MEMORY SYSTEM

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☐ c. Please debit Deposit Account No. 11-0600 in the amount of \$180.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 CFR §1.97(c)(2).


☐ 3. This Information Disclosure Statement is being filed after the mailing date of a final action, Notice of Allowance or an action that otherwise closes prosecution, but before payment of the Issue Fee. Applicant(s) hereby request(s) that the Information Disclosure Statement be considered. Please debit Deposit Account No. 11-0600 in the amount of \$180.00 in payment of the petition fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

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Respectfully submitted,

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STATEMENT BY APPLICANT**

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Sheet 1 of 2

**Complete if Known**

Application Number	Not assigned
Filing Date	
First Named Inventor	
Group Art Unit	Not assigned
Examiner Name	Not assigned
Attorney Docket Number	2207/16635

**U.S. PATENT DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	
		Number	Kind Code <sup>2</sup> (if known)			

**OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Wade et al, "Ovonyx Memory, Polymer Explored for Nonvolatile, Post-70-NM Generation", Intel Grooms Pair of Substitutes for Flash (Polymer Memory and Rewritable DVD-Like Approach Product Development, <u>Electrical Engineering Times</u> , July 16, 2001	
		Clarke, P, "Polymer Electronics Tapped for Memory, Logic" (Opticom ASA (Oslo, Norway) is developing a PC-card format polymer memory subsystem that should be completed before end 1999), <u>Electronic Engineering Times</u> , October 19, 1998	
		Stikeman, A., "Polymer Memory", <u>Technology Review</u> , Vol. 105, No. 7, September 2002	
		Stikeman, A., "Polymer Memory: The Plastic Path to Better Data Storage", <u>Technology Review</u> , Vol. 105, No. 7, September 2002	
		Sikora, A., "Developments in RAMs (random access memories): FeRAMS and MRAMS: Part 2", <u>Elektronik</u> , Vol. 51, No. 6 (Germany), March 19, 2002 (abstract)	
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		El-Kareh et al, "Field-Shielded Trench Fill", IBM Technical Disclosure Bulletin, Vol. 27, No. 8, January 1985 (abstract)	
		Jannson et al, "Optical Memory Based on the Ellipsometric Principle", 15th conference of the International Commission for Optics", Garmisch-Partenkirchen, Germany, August 5, 1990 (abstract)	
		Mayer, J., "Flash Memory Defends Its Crown" -- Pledging better performance, a pack of nonvolatile memory technologies is trying to unseat flash from its throne, but in this competitive market, cost is still king", <u>EBN</u> , No. 1338, pg. 29, 2002	
		Nagaraj, N., "Unfolding Space, Memory", <u>Business Line</u> , February 6, 2002	
		"Polymers News-Variable Resistivity Material for Memories", <u>Electronic Materials Technology News</u> , Vol. 3, No. 12, November 1989	

Examiner Signature		Date Considered	
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Sheet 2 of 2

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Group Art Unit	Not assigned
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		Number	Kind Code <sup>2</sup> (if known)			

### OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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		Wade, W., "Intel Details Post-Flash Technology Plan", <u>EE Times</u> , July 11, 2001, <a href="http://www.eetimes.com">www.eetimes.com</a> (11/27/02)	
		Lai, S., "Intel's Investigation of Next-Generation Memory Technologies for Portable Devices", Intel Corporation, TMG, California Technology and Manufacturing, July 2001	
		Avdeals.com, 28 pages of promotional materials	

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